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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/551,362 | 04/18/2000 | Yoshio Nagahiro | 1324.63957 | 2495 |

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Patrick G Burns Esq
Greer Burns & Crain Ltd
300 S. Wacker Dr.,
Suite 2500
Chicago, IL 60606

| EXAMINER |
|---|
| CHUNG, DAVID Y |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2871 | |

DATE MAILED: 02/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/551,362 | NAGAHIRO, YOSHIO | |
| | Examiner | Art Unit | |
| | David Y. Chung | 2871 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *10-13 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-13 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al. (U.S. 6,317,173) in further view of Moon (U.S. 5,942,310).

Jung discloses the following in column 1, lines 52 – 60: "A storage capacitor of the conventional polycrystalline silicon TFT-LCD includes a doped storage region in the silicon layer, a storage electrode overlapping the storage region and a gate insulating film interposed therebetween. Moreover, another storage capacitor is formed of the storage electrode, a pixel electrode overlapping the storage electrode and a dielectric including an interlayer insulating film and a passivation film interposed between the pixel electrode and the storage electrode." Jung discloses that storage capacitance wiring was conventional at the time of invention. See column 1, lines 15 – 20.

Jung does not teach a first and second insulating layer different from the gate insulator. Moon discloses a structure with insulating films having a dielectric constant larger than the gate insulator. Note in figure 2E, the storage capacitor formed by impurity doped semiconductor layer 2, storage electrode 4, and dielectric layer 6. Moon

teaches that with this type of structure, the capacitance level of the storage capacitor is increased. See column 4, lines 10 – 26. It would have been obvious to one of ordinary skill in the art at the time of invention to structure the conventional storage capacitors disclosed by Jung using insulating films different from the gate insulator in order to increase the storage capacitance and thereby improve the display quality.

2. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (U.S. 6,088,071) in further view of Moon (U.S. 5,942,310).

Note in figure 13 of Yamamoto, semiconductor layer 53a isolated from semiconductor layer 13, storage electrode 50b connected to storage line 50B, and pixel electrode 19 electrically connected to semiconductor layer 53a via contact electrode 50c formed in contact holes 55 and 57. See column 5, line 55 – column 6, line 15. A capacitor is formed between semiconductor layer 53a and storage electrode 50b via insulator 14. Another capacitor is formed between storage electrode 50b and pixel electrode 19 via insulator 18. Yamamoto discloses that electrode 53a may be doped with the same impurity as semiconductor layer 13. See column 5, line 63 – column 6, line 6. In this embodiment, the capacitance structure is formed in the middle of the pixel and the storage electrode is electrically connected to a separate storage line instead of the gate line. Otherwise, the embodiment of figure 13 is similar to that of figure 12.

Yamamoto does not teach a first and second insulating layer different from the gate insulator. Moon discloses a structure with insulating films having a dielectric constant larger than the gate insulator. Note in figure 2E, the storage capacitor formed

by impurity doped semiconductor layer 2, storage electrode 4, and dielectric layer 6. Moon teaches that with this type of structure, the capacitance level of the storage capacitor is increased. See column 4, lines 10 – 26. It would have been obvious to one of ordinary skill in the art at the time of invention to structure the storage capacitors disclosed by Yamamoto using insulating films different from the gate insulator in order to increase the storage capacitance and thereby improve the display quality.

3. Claims 12, 13 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima (U.S. 5,917,563) in further view of Ikeda et al. (U.S. 5,182,661).

Note in figures 8 and 9 of Matsushima, gate electrode 16a connected to gate line 16, source electrode 20a, drain electrode 21a, insulating film 50, upper electrode 51a connected to common wiring 51, first inter-layer insulating film 15, second inter-layer insulating film 24, and pixel electrode 25. A storage capacitor is formed of drain electrode 21a, insulating film 50, and upper electrode 51a. Another storage capacitor is formed of upper electrode 51a, second inter-layer insulating film 24, and pixel electrode 25. Matsushima discloses that the upper electrode 51a functions as a light-shielding layer. See column 15, lines 32 – 37.

Matsushima does not disclose a third storage capacitor formed of the drain electrode, first inter-layer insulating film, and gate line. Ikeda discloses a structure with a third storage capacitor between the first storage electrode and an extended portion of the gate line. See figures 4A and 4B. Ikeda teaches that forming additional capacitive elements can further increase the overall storage capacitance. See column 5, lines 55

– 65. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to form a third storage capacitor in the device of Matsushima by overlapping the drain electrode 21a and gate line 16 in order to increase the storage capacitance and thereby improve the display quality.

4. Claims 12, 13 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. 5,182,661) in further view of Jung et al. (U.S. 6,317,173).

Note in figures 4A and 4B, first storage capacitor electrode 60, second storage capacitor electrode 62, third storage capacitor electrode 68 connected to gate line 10, pixel electrode 22, insulator 42, insulator 44 and insulator 46. The first storage capacitor electrode is connected to the pixel electrode via contact hole 66. A first storage capacitor is formed between electrode 60 and electrode 62 via insulator 44. A second storage capacitor is formed between electrode 60 and pixel electrode 22 via insulator 46. A third storage capacitor is formed between electrode 60 and electrode 68 via insulator 42. The electrode 62 is formed of chromium and thus acts as a light-shielding film.

Ikeda discloses connecting storage capacitor electrode 62 to the gate line via contact holes instead of connecting them to a separate storage line. Jung teaches that both modes were conventional at the time of invention. See column 1, lines 15 – 20. It was well known and obvious that an electrically stable capacitor can be obtained by maintaining one of the capacitor electrodes at an appropriate potential. Furthermore, connecting electrode 62 to a separate storage line simplifies the manufacturing process

because both the capacitor electrodes and storage lines can be patterned in one step without the need to form contact holes in insulators 42 and 44. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to connect the second storage capacitor electrode of Ikeda to a separate storage line instead of the gate line in order to create a more stable capacitor and to simplify the manufacturing.

### *Response to Arguments*

Applicant's arguments with respect to claims 10, 11 and 12 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Chung whose telephone number is (703) 306-0155. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

David Chung
GAU 2871
01/25/03